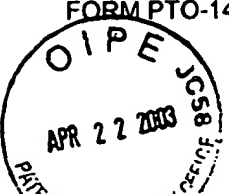


FORM PTO-1449 	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 174/221	APPLICATION NO. 09/924,274
		APPLICANT Paul Metzgen	CONFIRMATION NO. 4898
		FILING DATE August 7, 2001	GROUP 2422 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
VS	5,068,823	11/26/91	Robinson	395	500	
	5,142,625	08/25/92	Nakai	395	275	
	5,535,342	07/09/96	Taylor	395	307	
	5,548,228	08/20/96	Madurawe	326	41	
	5,684,980	11/04/97	Casselman	395	500	
	5,966,534	10/12/99	Cooke et al.	395	705	
	5,968,161	10/19/99	Southgate	712	37	
	6,085,317	07/04/00	Smith	713	1	
VS	6,282,627	08/28/01	Wong et al.	712	15	

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
VS	EP 0 419 105 A2	03/27/91	EPO	G06F	15/78		
	EP 0 419 105 A3	03/27/91	EPO	G06F	15/78		
	EP 0 445 913 A2	09/11/91	EPO	G06F	15/60		
	WO 94/10627	05/11/94	PCT	G06F	5/00		
	EP 0 759 662 A2	02/26/97	EPO	H03K	19/177		
	WO 97/09930	03/20/97	PCT	A61B	8/00		
	WO 97/13209	04/10/97	PCT	G06F	17/50		
	EP 0 801 351 A2	10/15/97	EPO	G06F	13/12		
	EP 0 801 351 A3	10/15/97	EPO	G06F	13/12		
	EP 0 829 812 A2	03/18/98	EPO	G06F	17/50		
VS	WO 00/38087	06/29/00	PCT	G06F	17/50		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

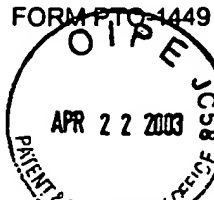
EXAMINER INITIAL	
VS	Callahan, Timothy J. et al. "The Garp Architecture and C Compiler," Computer, April 2000, pp. 62-69.
VS	Cardoso, J M P et al. "Macro-based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Proceedings of Seventh Annual IEEE Symposium, April 21, 1999, Los Alamitos, CA, pp. 2-11.

EXAMINER

VUTHE SIEK

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FORM PTO-1449 	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 174/221	APPLICATION NO. 09/924,274
		APPLICANT Paul Metzgen	CONFIRMATION NO. 4898
		FILING DATE August 7, 2001	GROUP 2122 2828

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
VS	Edwards, M.D. et al. "Software acceleration using programmable hardware devices," January 1996, pp. 55-63.
f	ELECTRONIK, DE, FRANZIS VERLAG GMBH - "MIT PROGRAMMIERBARER LOGIK VERHEIRATET," March 31, 1998, Vol. 47, No. 7, p. 38.
	Guccione, Steve. List of FPGA-based Computing Machines, < http://www.io.com/~guccione/HW_list.html >, Last Modified March 31, 1999.
	IBM, "Programmable Manual Cable Assembly Board," May 1989, IBM Technical Disclosure Bulletin, Vol. 31, pp. 306-309.
	Iseli et al. "A C++ compiler for FPGA custom execution synthesis," <u>Proceedings of IEEE Symposium</u> , April 19, 1995, Los Alamitos, CA, pp. 173-179.
	Isshiki, T et al. "Bit-serial pipeline synthesis and layout for large-scale configurable systems," <u>Proceedings of The ASP-DAC '97</u> , January 28, 1997, Chiba, Japan, pp. 441-446.
	Kastrup, Bernardo et al. "ConCISe: A Compiler-Driven CPLD-Based Instruction Set Accelerator," <u>Proceedings of Seventh Annual IEEE Symposium</u> , April 21, 1999, Los Alamitos, CA, pp. 92-101.
	Nanya, T. "Asynchronous VSLI System Design," ASP-DAC '98 Tutorials, February 10, 1998, Yokohama, Japan.
	Nanya, T. et al. "Scalable-Delay-Insensitive Design: A high-performance approach to dependable asynchronous systems," <u>Proceedings of International Symposium on Future of Intellectual Integrated Electronics</u> , March, 1999, pp. 531-540.
	Page, Ian. "Constructing Hardware-Software Systems from a Single Description," <u>Journal of VSLI Signal Processing</u> , vol. 12, no. 1, January, 1996, pp. 87-107.
	Semeria, L. et al. "SpC: synthesis of pointers in C application of pointer analysis to the behavioral synthesis from C," <u>Proceedings of ICCAD International Conference on Computer Aided Design</u> , November 8-12, 1998, San Jose, CA, pp. 340-346.
	Wazlowski, M. et al. "PRISM-II compiler and architecture," <u>Proceedings of IEEE Workshop</u> , April 5, 1994, Los Alamitos, CA, pp. 9-16.
	Wirthlin, Michael J. et al. "Improving Functional Density Using Run-Time Circuit Reconfiguration," <u>IEEE Transactions on Very Large Scale Integration (VSLI) Systems</u> , Vol. 6, No. 2, June 1998, pp. 247-256.
VS	Wo, D. et al. "Compiling to the gate level for a reconfigurable co-processor," <u>Proceedings of IEEE Workshop</u> , April 10, 1994, Los Alamitos, CA, pp. 147-154.

All references have been considered

Examiner

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